## REMARKS

Claims 1-14 and 17-20 remain in the present application. Claims 1-20 are rejected. Claims 15 and 16 are cancelled. Although Claim 14 is amended herein, Applicants respectfully submit that no new matter has been added by the claim amendments. Applicants respectfully request further examination and reconsideration of the rejections based on the amendments and arguments set forth below.

### Provisional Double Patenting Rejection

The above referenced Office Action cites a provisional rejection of independent Claims 1, 7 and 14. Applicants will respond to the provisional double patenting rejection upon an indication of allowance of subject matter from either the present application or the co-pending application (09/975,338).

### Claim Rejections - 35 U.S.C. §103

The above referenced Office Action rejects Claims 1-20 as being unpatentable over U.S. Patent No. 5,748,875 (hereafter referred to as "Tzori") in view of "Debugging with The GNU Source-Level Debugger" by Richard M. Stallman and Roland H. Pesch (hereafter referred to as "Stallman"). Applicants respectfully traverse.

Applicants respectfully direct the Examiner to independent Claim 1 that recites an In-Circuit Emulation system breakpoint control, comprising (emphasis added):

> a microcontroller;
> a virtual microcontroller operating in lock-step synchronization with the microcontroller;
> a breakpoint lookup table associated with the virtual microcontroller with a break bit associated with each of a plurality of instruction addresses, the break bit being set to indicate that a break is to occur at a specified instruction address; and
> a breakpoint controller that sends a break message to the microcontroller whenever an instruction address is encountered that is associated with a set break bit.

Independent Claims 7 and 14 recite limitations similar to those in Claim 1. Claims 2-6 depend from independent Claim 1 and recite further limitations to the claimed invention. Claims 8-13 depend from independent Claim 7 and recite further limitations to the claimed invention. Claims 15-20 depend from independent Claim 14 and recite further limitations to the claimed invention.

Applicants respectfully assert that Tzori fails to suggest, teach, or describe the limitations of "a virtual microcontroller operating in lock-step synchronization with the microcontroller" as recited in Claim 1. Specifically, as described in lines 1-8 of page 17 of the application as filed, the phrase "lock-step synchronization" should be understood as follows:

> Synchronization between the microcontroller 232 and the virtual microcontroller 220 is achieved by virtue of their virtually identical operation. They are both started simultaneously by a power on or reset signal. They then track each other's operation continuously executing the same instructions using the same clocking signals. The system clock signal and the microcontroller clock signal are shared between the two microcontrollers (real and virtual) so that even if the microprocessor clock is changed during operation, they remain in lock-step.

In contrast, Applicants understand Tzori to teach a digital logic simulator coupled to a hardware pod for carrying out stimulation-response cycles (Abstract; Figure 1). More specifically, as shown in the timing diagram of Figure 3, Tzori teaches that the stimulation-response cycles involve independent operation of the simulator (e.g., as shown in Figure 3, from vertical line 106 to 108, and from vertical line 128 to the end of the simulation cycle) and the hardware pod (e.g., as shown in Figure 3, from vertical line 108 to 128). However, this is very different from the invention as claimed. For example, even assuming arguendo that the hardware pod is a microcontroller as claimed, the simulator and hardware pod do not operate in lock-step synchronization as claimed. Instead, the simulator and hardware pod operate independently, as shown by Figure 3 and discussed previously. Moreover, by teaching independent operation, Tzori effectively teaches away from the claimed embodiments directed to lock-step synchronization.

Furthermore, the deficiencies of Tzori are not cured by Stallman. Applicants respectfully assert that Stallman also fails to suggest, teach, or describe the limitations of "a virtual microcontroller operating in lock-step synchronization with the microcontroller" as recited in Claim 1.

Applicants respectfully assert that Tzori fails to suggest, teach, or describe the limitations of "a break bit associated with each of a plurality of instruction addresses" and "the break bit being set to indicate that a break is to occur at a specified instruction address" as recited in Claim 1. As described in reference to Figure 8, embodiments of the claimed invention involve inspecting a breakpoint table stored in a virtual microcontroller for a set break bit associated with an instruction, such that a break message may be sent to a microcontroller to implement a break in instruction execution (line 25 of page 26 through line 7 of page 27).

In contrast, Tzori teaches a digital logic simulator without the use of breakpoints, break bits, or the like. As such, Applicants respectfully assert that Tzori fails to suggest, teach, or describe the limitations of "a break bit associated with each of a plurality of instruction addresses" and "the break bit being set to indicate that a break is to occur at a specified instruction address" as recited in Claim 1.

Furthermore, the deficiencies of Tzori are not cured by Stallman. Applicants understand Stallman to teach setting breakpoints with a break command or its variants to specify places where a program should stop by line number, function name, or exact address in the program (page 1 of 13). For example, on page 3 of 13, Stallman teaches: "Address; Where the breakpoint is in your program, as a memory address; What; Where the breakpoint is in the source for your program, as a file and line number." However, Stallman fails to suggest, teach, or describe the use of break bits associated with instruction addresses and stored in a breakpoint lookup table to effectuate an instruction break as claimed. Moreover, by teaching breakpoints without the use of break bits as claimed, Stallman effectively teaches away from the claimed embodiments.

Applicants respectfully assert that Tzori fails to suggest, teach, or describe the limitations of "a breakpoint controller that sends a break message to the microcontroller whenever an instruction address is encountered that is associated with a set break bit" as recited in Claim 1. As discussed above, Tzori teaches a digital logic simulator without the use of breakpoints, break bits, or the like. Consequently, Tzori also fails to teach a breakpoint controller that sends a break message to the microcontroller whenever an instruction address is encountered that is associated with a set break bit.

Furthermore, the deficiencies of Tzori are not cured by Stallman. As discussed above, Stallman is silent regarding break bits with associated instruction addresses. Consequently, Stallman also fails to suggest, teach, or describe the limitations of "a breakpoint controller that sends a break message to the microcontroller whenever an instruction address is encountered that is associated with a set break bit" as recited in Claim 1. Moreover, by teaching breakpoints without the use of break bits or a break bit controller as claimed, Stallman effectively teaches away from the claimed embodiments.

Furthermore, independent Claim 14 has been amended herein to include the limitations "at each instruction of the sequence of instructions, inspecting the breakpoint lookup table for a set break bit associated with instruction" and "halting execution of instructions in the microcontroller and the virtual microcontroller prior to the instruction associated with the set break bit." Applicants respectfully submit that neither Tzori nor Stallman suggest, teach, or describe either of these limitations as claimed, given that both Tzori and Stallman fail to teach the use of break bits associated with instruction addresses as discussed above.

For these reasons, Applicants respectfully assert that independent Claims 1, 7, and 14 are not rendered obvious by Tzori in view of Stallman. Since Claims 2-6 depend from independent Claim 1, Claims 8-13 depend from independent Claim 7, and Claims 17-20 depend from independent Claim 14, the dependent Claims are also not rendered obvious by Tzori in view of Stallman. Thus, Claims 1-14 and 17-20 overcome the 35 U.S.C. §103(a) rejections of record, leaving these claims in a state of allowance.

## CONCLUSION

Based on the arguments presented above, Applicants respectfully assert that Claims 1-14 and 17-20 overcome the rejections of record. Therefore, Applicants respectfully solicit allowance of these Claims.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

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